



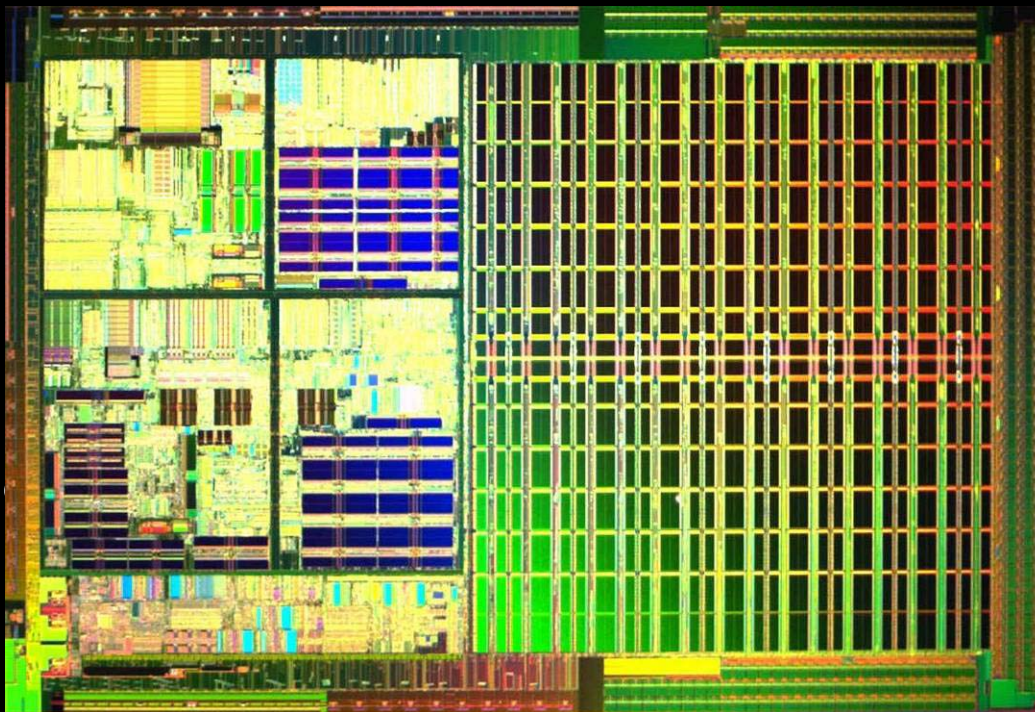
William Siegle
SVP, Chief Scientist
November 6, 2003

90 nm MPUs

Ready for 2004!

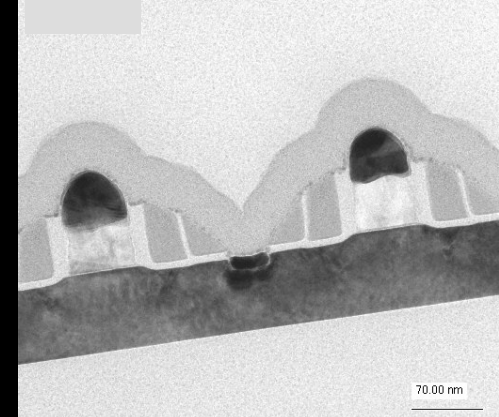


- 90 nm AMD64 in active pilot mode in Fab 30.
- Prototype parts running in systems.

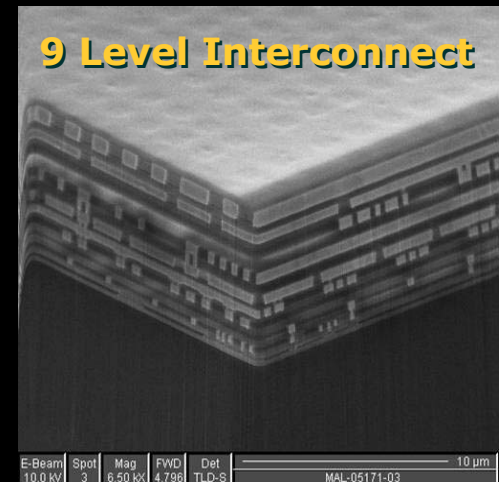


114 mm² AMD Opteron™ processor die in 90 nm

Transistor For 90 nm



9 Level Interconnect



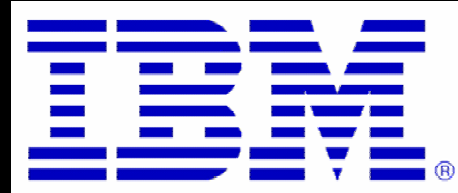
E-Beam	Spot	Mag	FWD	Det	
10.0 kV	3	6.50 kX	4.796	TLD-S	
					MAL-05171-03



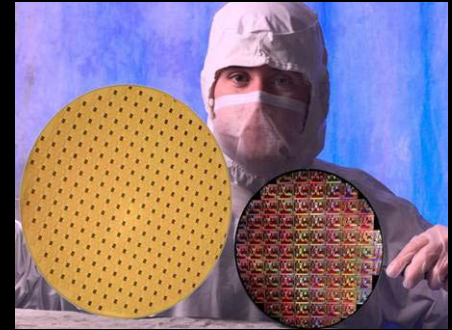
2003 Analyst Day

IBM Joint Development

A World Class Team with Common Goals



- Joint development with IBM implemented in January 2003
 - Team in place and growing
- Program through qualification of 65 nm, and early work on 45 nm generation
- Joint team at IBM 300 mm development/manufacturing facility in East Fishkill, NY
- World class team, facility and equipment
- Common goals in high performance



Memory Development

Cranking Up the Pace!

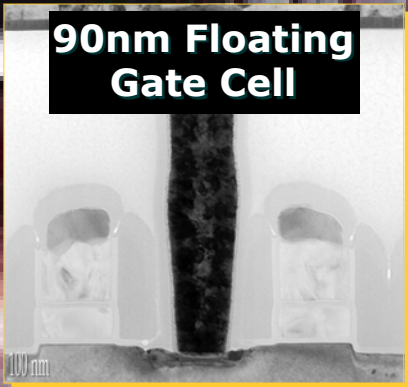


Implementation of IBM JDA for logic enables AMD's SDC to focus on accelerating memory technology

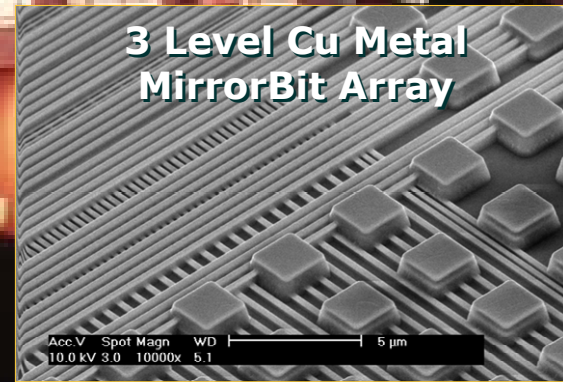
90 nm floating gate and MirrorBit™ devices in development

First use of Cu interconnect on Flash products

90nm Floating Gate Cell



3 Level Cu Metal MirrorBit Array



Transistor Research

Inventing the Future!



IEDM 1999
(90 nm node*)



Lg=50 nm

AMD's transistor among the industry's smallest & fastest

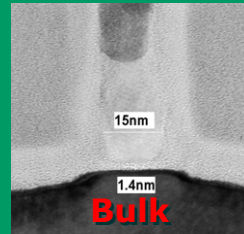
VLSI 2001
(65 nm node*)



Lg=35 nm

AMD again achieves one of the smallest & fastest transistors

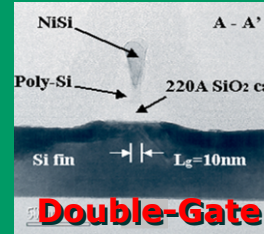
IEDM 2001
(32 nm node*)



Lg=15 nm

AMD achieves the world's fastest transistor

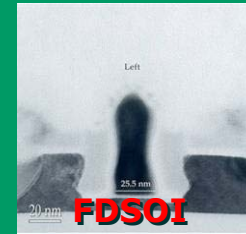
IEDM 2002
(22 nm node*)



Double-gate Lg=10 nm

AMD creates the world's smallest double-gate (3-D)

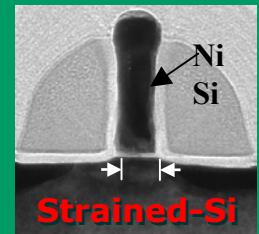
VLSI 2003
(65 nm node*)



Metal Gate Lg=25 nm

AMD achieves the industry's fastest P-channel FDSOI device.

VLSI 2003
(65 nm node*)



Metal Gate Lg=35 nm

AMD achieves superior performance using Strained-Si and Metal Gates.



2003 Analyst Day

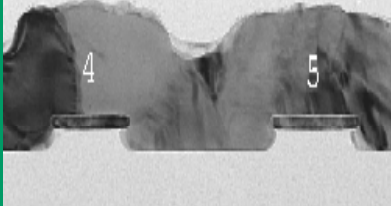
Transistor Research

Inventing the Future!



SSDM 2003

Triple-Gate



**Multi-gate structure
L_g=20nm**

**AMD research
transistors
surpass ITRS
2009
performance
projections**

- **This work combines the key innovations from the previous research:**
 - Ultra-thin, FDSOI
 - Metal gate (NiSi)
 - Intrinsic channels
 - Selective epi
 - Multi-gate 3D structure
 - Strain engineering
- **Advantages:**
 - Lower leakage (Off current and gate leakage)
 - Higher drive currents
 - Faster switching
 - Conventional materials/processes
 - Greater compatibility with current design techniques

Advanced Mask Technology Center

Photomasks Through Collaboration



- Joint Venture of AMD, Inc., Infineon Technologies AG, and DuPont Photomasks, Inc.
- Investments of about € 360 million
- Approximately 170 jobs
- Construction start: June 2002

- Established to become a world-leading facility for the development and pilot manufacturing of advanced photomasks
- Grand opening October 13, 2003
- First photomasks October 2003



Delivering on the Promise

AMD64 in April and September

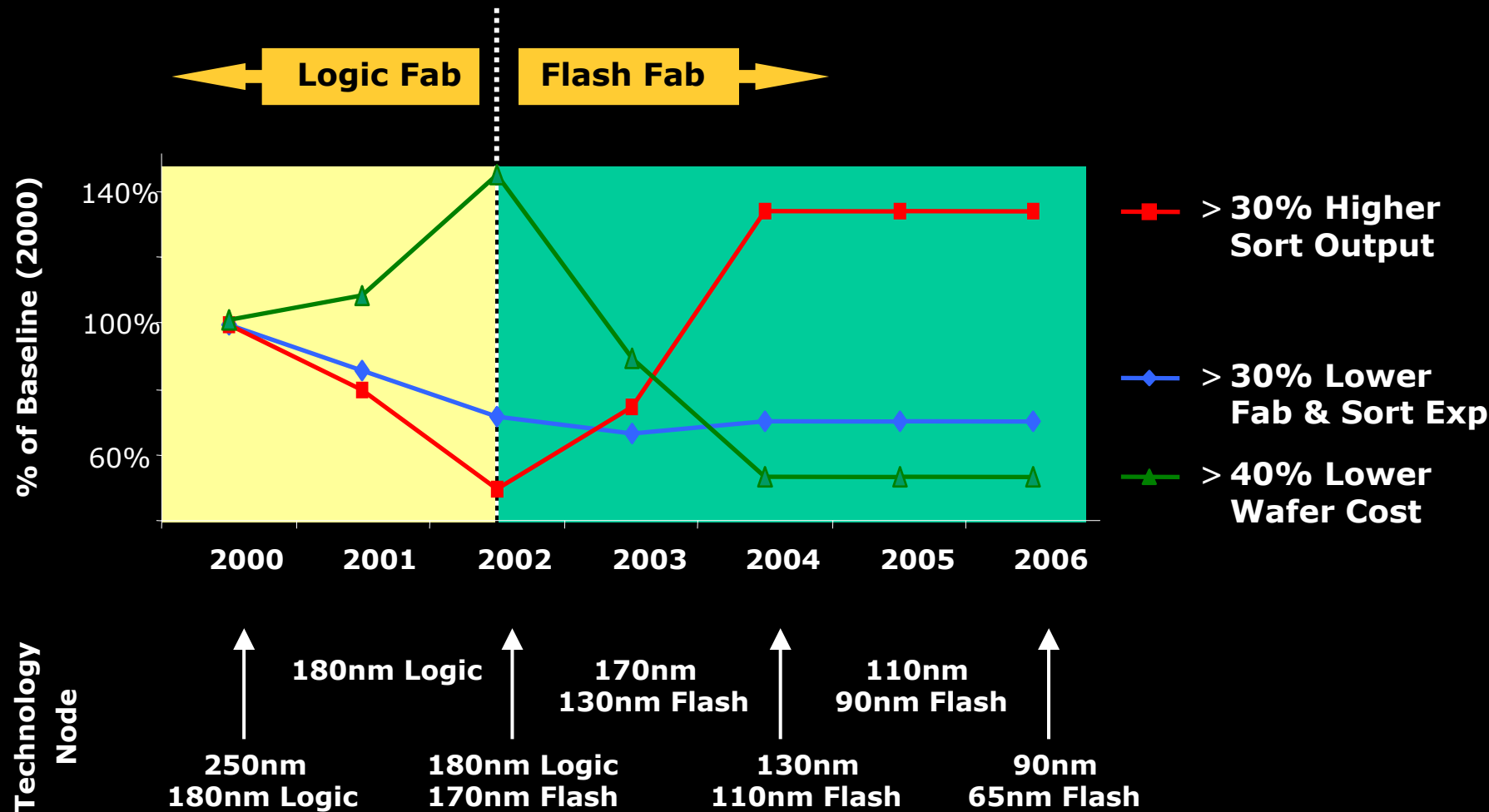


- **Mature 130 nm production — bulk and SOI processes**
- **AMD Opteron™ processor and AMD Athlon™ 64 processor introduced and running mature yields**
- **90 nm ready for 2004 conversion**

Fab 30 Production

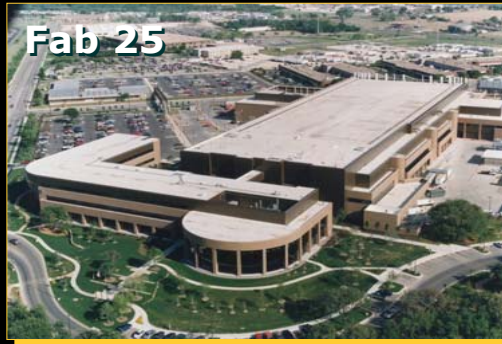


Fab 25 World Class Execution

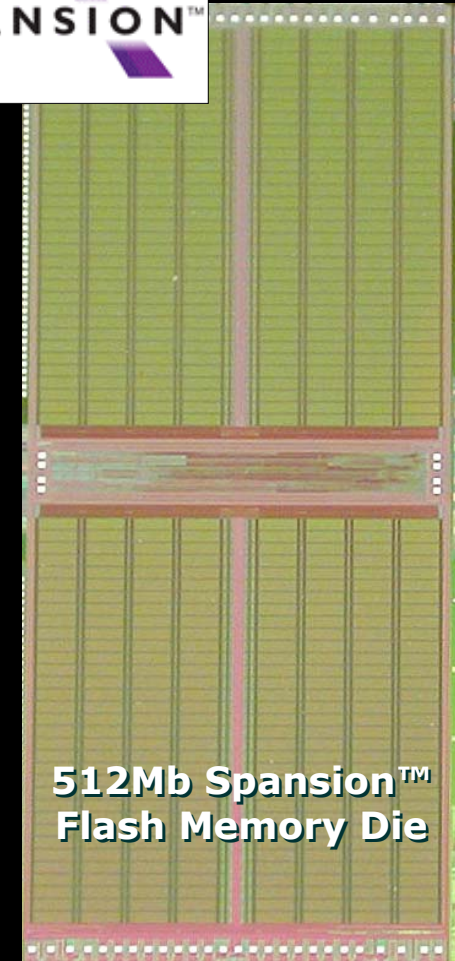


Memory Production

Strength Through Consolidation



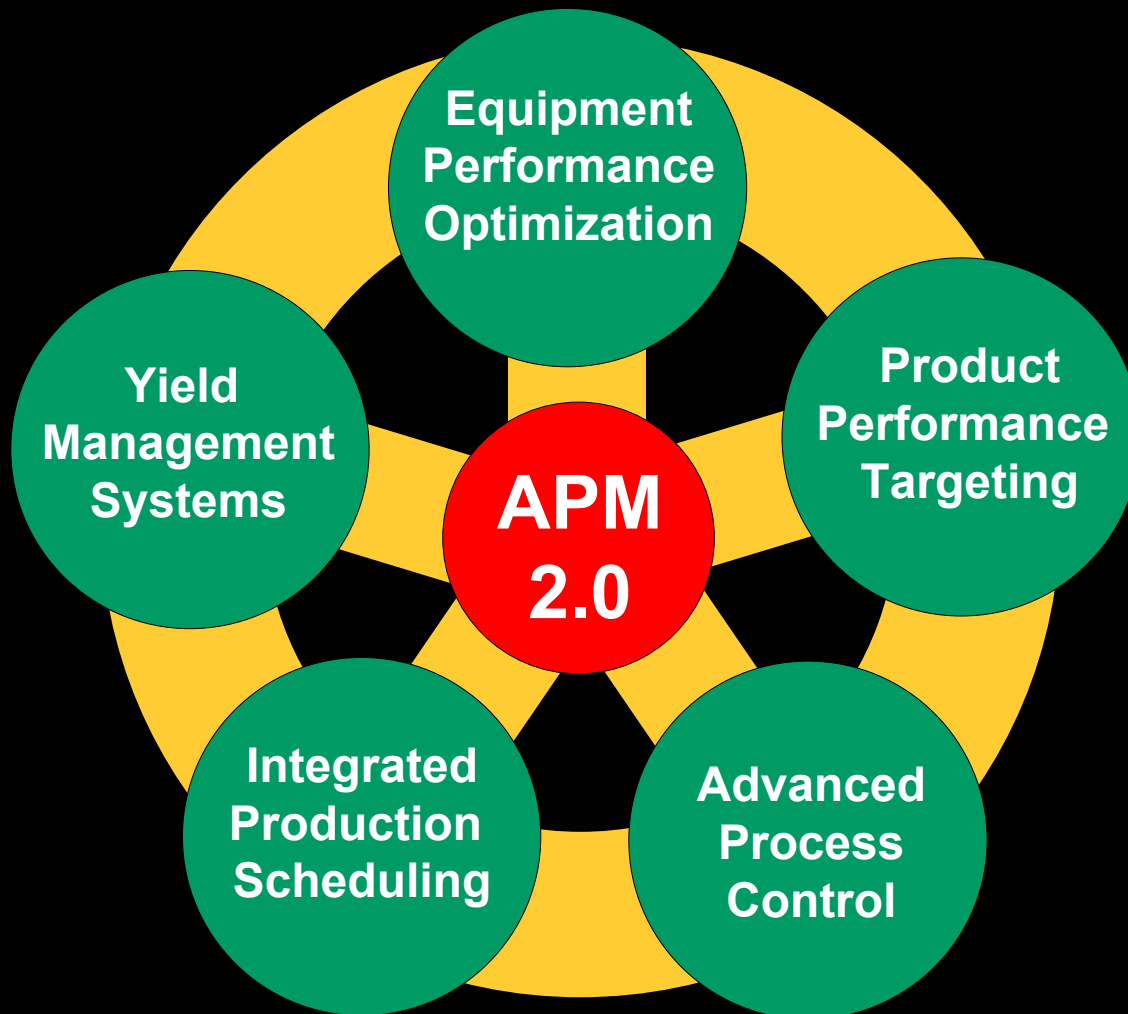
- Fab 25 successfully completes transition from MPU to Flash fab
- FASL LLC (Spansion™) implementation represents >10,000 wafers per week capacity at ≤ 180 nm design rules in Fab 25 and JV3
- 130 nm in production since early '03 (floating gate), MirrorBit™ in volume production, 130 nm 512 Mb device in sampling
- JV1/2 supporting volume ramp of MirrorBit



**512Mb Spansion™
Flash Memory Die**

AMD Automated Precision Manufacturing **AMD**

Enabling World Class Execution



- *Highly Automated, Integrated Decision Making*
- *Non-Stop Cycle of Improvement*
- *Maximum Efficiency*

AMD Fab 30 is best* in five out of eight key efficiency areas in Q1'03

BEST

Photo
Alignments
Per Photo
Aligner

BEST

Photo
Alignments
Per Scanner
Per Day -
DUV

BEST

Copper
Plating Outs
Per Day Per
System

BEST

Copper CMP
Outs Per Day
Per System

BEST

CVD ILD Outs
Per Day
Per System

* Based on SEMATECH's standardized benchmarking process, which compared SEMATECH member Q1'03 fab performance submissions against verified member data from Q4'02.

AMD Fab 30 yields are best* in Q2'03:



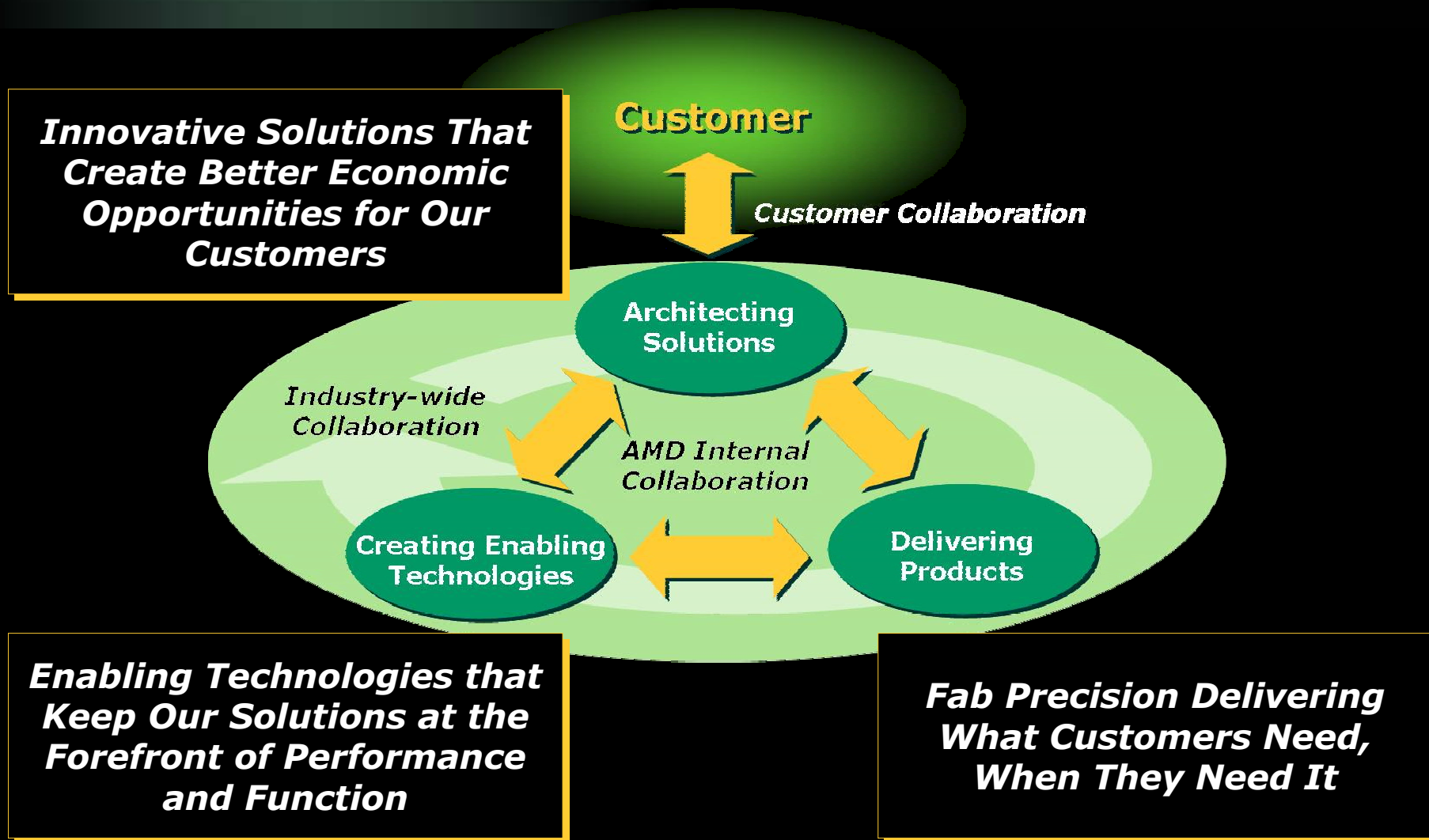
* Based on SEMATECH's standardized benchmarking process, which compared SEMATECH member Q2'03 fab performance submissions against verified member data from Q1'03.

Strengthening Our Hand for 2004!



- AMD64 launched and ramped
 - Achieving mature yields on all 130 nm products
- Fab 25 (fully converted) joins Aizu JV3 for Flash
 - Capacity for high density products
- APM widely deployed in Fab 30 and Fab 25
 - Enabling high productivity and precision execution
- 90 nm preparing for production
 - AMD64 products in 2004; prototypes now
 - Accelerated development for Flash, Floating Gate and MirrorBit™
- IBM joint development
 - Focus on 65 nm, 300 mm node for 2005/6
- Leading edge research
 - Continuing efforts in devices, materials and lithography
- Networks of collaboration

Customer Centric Technology Strategy



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